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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,502	06/23/2003	Chengting Zhao	P16304	9693

28062 7590 10/05/2006

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,502	ZHAO ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8,10-12,15-21 and 24-29* is/are rejected.

7)☒ Claim(s) *4-6,9,13,14,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending.

Claim Objections

2. Claim 24 is objected to because of the following informalities: there is a period before the comma in the first line of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 7-8, 10-12, 15-21 and 24-29 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 4,218,742 to Carlton et al.

5. As to claim 1, Carlton discloses a device comprising: a synchronization circuit [52, 62] to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal [51], and to generate a load signal based on the synchronized synchronization signal [col. 4, lines 11-22]; and a ring counter [BIT RING] to receive the load signal from the synchronization circuit and to circularly propagate the load signal [col. 3, lines 58-68 and col. 4, lines 1-2].

6. As to claim 2, Carlton discloses an enabling circuit [28] to assert and to deassert an enable signal, wherein the ring counter is to receive the enable signal, to receive the load signal from the synchronization circuit [62] if the enable signal is asserted, and to circularly propagate the load signal if the enable signal is deasserted [col. 4, lines 19-22].

7. As to claim 3, Carlton discloses a circuit to detect whether a load pulse within the load signal has been received by the ring counter, and to deassert the enable signal if the load pulse has been received by the ring counter [col. 3, lines 50-57].

8. As to claim 7, Carlton discloses a multiplexer [60] to receive the load signal from the synchronization circuit [62], to receive a circularly propagating load signal from the ring counter [BIT RING 0-7], to receive an enable signal [DISABLE SBD], to output the received load signal to the ring counter if the enable signal is asserted, and to output the circularly propagating load signal to the ring counter if the enable signal is deasserted [col. 4, lines 2-10].

9. As to claim 8, Carlton discloses an enabling circuit [62] to detect whether a load pulse of the load signal has been received by the ring counter, and to deassert the enable signal only if the load pulse has been received by the ring counter [col. 4, lines 2-10].

10. As to claim 10, Carlton discloses a method comprising: receiving a synchronization signal, the synchronization signal substantially synchronized with a data transition [col. 4, lines 11-22]; synchronizing the synchronization signal with a clock signal [col. 3, lines 58-64 and col.

4, lines 11-22]; generating a load signal based on the synchronized synchronization signal, the load signal including a load pulse [col. 4, lines 11-22]; inputting the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to a minimum data transition period [col. 3, lines 58-68 and col. 4, lines 1-2]; and outputting the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the data transition period [col. 1, lines 12-22].

11. As to claim 11, Carlton discloses the synchronization signal is synchronized with a data signal, the data signal reflecting the minimum data transition period [col. 3, lines 58-64].

12. As to claim 12, Carlton discloses the period of the synchronization signal is substantially equal to the data transition period [col. 4, lines 11-22].

13. As to claim 15, Carlton discloses outputting the load signal from the ring counter comprises: receiving a plurality of load signals from the ring counter, at least one of the plurality of load signals being delayed with respect to at least one other of the plurality of load signals [col. 1, lines 18-22]; selecting one of the plurality of load signals to output [col. 3, lines 58-68 and col. 4, lines 1-2]; and outputting the selected load signal [col. 3, lines 58-68 and col. 4, lines 1-2].

14. As to claim 16, Carlton discloses a load pulse of the selected load signal is substantially synchronized with a center of the data eye [col. 1, lines 18-22]. Carlton teaches that the content of each bit is clocked out, not that its transition.

15. As to claim 17, Carlton discloses selecting one of the plurality of load signals comprises: receiving an offset signal; and selecting a load signal output from one of the one or more delay elements based on the offset signal [col. 3, lines 58-68 and col. 4, lines 1-2].

16. As to claim 18, Carlton discloses inputting the load signal comprises: asserting an enable signal to input the load signal into the ring counter, and further comprising: deasserting the enable signal to shift the load signal through the ring counter [col. 4, lines 2-10].

17. As to claim 19, Carlton discloses a device to: receive a synchronization signal, the synchronization signal substantially synchronized with a minimum data transition period [col. 4, lines 11-22]; synchronize the synchronization signal with a clock signal [col. 3, lines 58-68 and col. 4, lines 1-2]; generate a load signal based on the synchronized synchronization signal, the load signal including a load pulse [col. 4, lines 11-22]; input the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to the minimum data transition period [col. 1, lines 18-22]; and output the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the minimum data transition period [col. 1, lines 18-22].

18. As to claim 20, Carlton discloses the synchronization signal to be synchronized with a data signal, the data signal to reflect the minimum data transition period [col. 3, lines 58-64 and col. 4, lines 11-22].

19. As to claim 21, Carlton discloses the period of the synchronization signal to be substantially equal to the data transition period [col. 4, lines 11-22].

20. As to claim 24, Carlton discloses output of the load signal from the ring counter comprises: reception of a plurality of load signals from the ring counter, at least one of the plurality of load signals to be delayed with respect to at least one other of the plurality of load signals [col. 1, lines 18-22]; selection of one of the plurality of load signals to output [col. 3, lines 58-68 and col. 4, lines 1-2]; and output of the selected load signal [col. 3, lines 58-68 and col. 4, lines 1-2].

21. As to claim 25, Carlton discloses a load pulse of the selected load signal is substantially synchronized with a center of the data eye [col. 1, lines 18-22]. Carlton teaches that the content of each bit is clocked out, not that its transition.

22. As to claim 26, Carlton discloses selecting one of the plurality of load signals comprises: receiving an offset signal; and selecting a load signal output from one of the one or more delay elements based on the offset signal [col. 3, lines 58-68 and col. 4, lines 1-2].

23. As to claim 27, Carlton discloses inputting the load signal comprises: asserting an enable signal to input the load signal into the ring counter, and further comprising: deasserting the enable signal to shift the load signal through the ring counter [col. 4, lines 2-10].

24. As to claim 28, Carlton discloses a system comprising: a memory controller hub comprising: a synchronization circuit [52, 62] to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal [51], and to generate a load signal based on the synchronized synchronization signal [col. 4, lines 11-22]; a ring counter [BIT RING] to receive the load signal from the synchronization circuit and to circularly propagate the load signal [col. 3, lines 58-68 and col. 4, lines 1-2]; and a parallel-to-serial converter [50] to generate serial data based on the load signal [col. 4, lines 23-29]. It is well known in the art that the serial data from a serial data channel device can be forwarded to portions of the system receiving serial data [col. 1, lines 8-10], such as from a memory hub to a double-rate memory.

25. As to claim 29, Carlton discloses the ring counter comprises one or more delay elements to receive the load signal, to delay the load signal, and to output the delayed load signal [col. 1, lines 12-23], and wherein the memory controller hub further comprises a multiplexer to receive a delayed load signal from a plurality of the one or more delay elements, to receive an offset signal, and to output one of the received delayed load signals based on the offset signal [col. 3, lines 58-68 and col. 4, lines 1-2].

Allowable Subject Matter

26. Claims 4-6, 9, 13-14 and 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 12, 2006
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